AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A data packet switching node to be used in an asynchronous digital network, comprising:

[[-]] an input stage, cutting data packets into segments of constant length;[[,]]

[[-]] a switching matrix for switching, said switching matrix having input ports and output ports supporting identical bit rates B; and

[[-]] ~~and~~ an output stage reconstructing said data packets from said segments supplied by said output ports of said switching matrix, wherein

[[-]] said input stage comprises at least one input interface with a bit rate equal to a multiple of B, ki*B, and means for splitting data packets received on said interface into segments distributed to ki input ports of said switching matrix;

[[-]] said output stage comprises at least one output interface with a bit rate equal to a multiple of B, ko*B, and means for reconstructing a data packet with a bit rate equal to ko*B by concatenating segments supplied by ko output ports of said switching matrix; and

[[-]] ki*ko>1.

2. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 1, said switching matrix further comprising:

[[-]] a first memory location for storing an identifier representing the association between said input interface and said corresponding ki input ports; and

[[-]] a second memory location for storing an identifier representing the association between said output interface and said corresponding ko output ports.

3. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 1, said switching matrix further comprising:

[[-]] a buffer memory for storing segments belonging to a packet received at said input interface,

[[-]] memory writing means for sequentially writing segments received on said ki input ports in said buffer memory;

[[-]] a translation table for determining the output interface to which said segments belonging to said packet must be switched;

[[-]] a traffic management module for storing the address of the first segment of said packet in said buffer memory; and

[[-]] memory reading means for retrieving consecutive segments belonging to said packet in said buffer memory and cyclically assigning each of said segments to one of said ko output ports associated to said output interface.

4. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 1, dedicated to be used in an ATM switch to switch fixed length data packets supplied on said input interface.

5. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 1, dedicated to be used in an IP router to switch variable length data packets supplied on said input interface.

6. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 1, dedicated to be used in an equipment providing both IP routing and ATM switching functions.

7. (*Currently Amended*) The ~~A~~ data packet switching node according to claim 2, wherein the association between each input interface and corresponding input ports, as well as the association between each output interface and corresponding output ports are dynamically configurable in said first and second memory location.

8. (*New*) The data packet switching node according to claim 1, said switching matrix further comprising:

a buffer memory for storing segments belonging to a packet received at said input interface,

a memory write circuit for sequentially writing segments received on said ki input ports in said buffer memory;

a translation table for determining the output interface to which said segments belonging to said packet must be switched;

a traffic management module for storing the address of the first segment of said packet in said buffer memory; and

a memory read circuit for retrieving consecutive segments belonging to said packet in said buffer memory and cyclically assigning each of said segments to one of said ko output ports associated to said output interface.

9. (*New*) The data packet switching node according to claim 1, wherein variable length data packets are cut into segments of identical length, and, if necessary, the last segment of a variable length packet is filled with dummy bits so as to equalize the length of all the segments.

10. (*New*) A data packet switching node to be used in an asynchronous digital network, comprising:

an input stage, cutting data packets into segments of constant length;

a switching matrix for switching, said switching matrix having input ports and output ports supporting identical bit rates B;

a buffer memory for storing segments of a packet received at said input stage, wherein a memory location for storing segments is based on a clock period as measured from receipt of an initial segment and the modulo of the number of input ports of said switching matrix; and

an output stage reconstructing said data packets from said segments supplied by said output ports of said switching matrix, wherein

said input stage comprises at least one input interface with a bit rate equal to a multiple of B, ki*B, and means for splitting data packets received on said interface into segments distributed to ki input ports of said switching matrix;

said output stage comprises at least one output interface with a bit rate equal to a multiple of B, ko*B, and means for reconstructing a data packet with a bit rate equal to ko*B by concatenating segments supplied by ko output ports of said switching matrix; and

ki*ko>1.

11. (*New*) The data packet switching node according to claim 10, said switching matrix further comprising:

a first memory location for storing an identifier representing the association between said input interface and said corresponding ki input ports; and

a second memory location for storing an identifier representing the association between said output interface and said corresponding ko output ports.

12. (*New*) The data packet switching node according to claim 10, said switching matrix further comprising:

a memory write circuit for sequentially writing segments received on said ki input ports in said buffer memory;

a translation table for determining the output interface to which said segments belonging to said packet must be switched;

a traffic management module for storing the address of the first segment of said packet in said buffer memory; and

a memory read circuit for retrieving consecutive segments belonging to said packet in said buffer memory and cyclically assigning each of said segments to one of said ko output ports associated to said output interface.

13. (*New*) The data packet switching node according to claim 10, dedicated to be used in an ATM switch to switch fixed length data packets supplied on said input interface.

14. (*New*) The data packet switching node according to claim 10, dedicated to be used in an IP router to switch variable length data packets supplied on said input interface.

15. (*New*) The data packet switching node according to claim 10, dedicated to be used in an equipment providing both IP routing and ATM switching functions.

16. (*New*) The data packet switching node according to claim 11, wherein the association between each input interface and corresponding input ports, as well as the association between each output interface and corresponding output ports are dynamically configurable in said first and second memory location.

17. (*New*) A method for operating a data packet switching node comprising a switching matrix having input ports and output ports supporting identical bit rates B, an input stage comprising at least one input interface with a bit rate equal to a multiple of B, and an output stage comprising at least one output interface with a bit rate equal to a multiple of B, said method comprising:

cutting input data packets into segments of constant length;

distributing split data packets to ki input ports of said switching matrix;

switching segments within said switching matrix; and

reconstructing a data packet by concatenating segments supplied by ko output ports of said switching matrix, wherein ki*ko>1.

18. (*New*) The method according to claim 17, said method further comprising:

storing, in a first memory location, an identifier representing the association between said input interface and said corresponding ki input ports; and

storing, in a second memory location, an identifier representing the association between said output interface and said corresponding ko output ports.

19. (*New*) The method according to claim 18, wherein the association between each input interface and corresponding input ports, as well as the association between each output interface and corresponding output ports are dynamically configurable in said first and second memory location.

20. (*New*) The method according to claim 17, wherein variable length data packets are cut into segments of identical length, and, if necessary, the last segment of a variable length packet is filled with dummy bits so as to equalize the length of all the segments.